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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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1515 MARKET STREET
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EXAMINER	
CHANG, EDITH M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,093	CHEN ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,27 and 31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,27 and 31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 15, 2004 have been fully considered but they are not persuasive.

Claims 1 and 16 in page 8 lines 22-25, Applicants argue that the reference (Zhou) does not teach shift registers. In the Abstract lines 2-6, Zhou teaches the shift register used in the match filter circuit.

Claims 33 and 35 in page 9 lines 13-15 and lines 34-36, Applicants argue that the reference does not teach an output from each stage of first and second shift registers being multiplied by an associated, respective tap weight. In FIG.3, it clearly indicates that the each stage of the first and second shift registers being multiplied by an associated respective tap weight (PN) on CLK0 and CLK1 respectively, hence teaches the steps cited in the claims.

Claim Objections

2. Claims 38-46 objected to because of the following informalities:

Claims 38 & 46, lines 9 & 12: "the shift registers" is suggested changed to "the N multiple-stage shift registers"

Claim 42, line 2; Claim 43, line 3 & Claim 45, line 2: "the shift registers" is suggested changed to "the N multiple-stage shift registers".

Claims 39-41 and 43-45 are directly or indirectly dependent on the objected claim 38.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-15 and 16-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims1 and 16, the disclosure of the drawings teaches *a sum output* generated by the ADDER, does not teach *two or more sum outputs* are generated.

Claims 2-15 and 17-32 are directly or indirectly dependent on the rejected claims 1 and 16.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-32 and 38-46 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 16, line 13: "the shit registers" lacks antecedent basis.

Claims 38 & 46, line 11: "each set of data" lacks antecedent basis.

Claim 44, line 1: "the shift registers" lacks antecedent basis.

Claims 2-15, 17-32 and 39-43 and 45 are directly or indirectly dependent on the rejected claims 1, 16 and 38.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 4-5, 12, 16, 19-20, 27, 33, 35-36 and 38-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (US 6625205 B1).

Regarding **claims 1, 12, 16 & 27**, in Fig.23, Zhou et al. teaches digital filter /a receiver including a digital filter (column 1 lines 5-15 wherein the reception apparatus is the receiver), comprising: at least two multiple stage shift registers (Fig.23 SFREG1 & SFREG2 with n stages); a plurality of multiplier corresponding in number to the number of stages in the at least two multiple stage shift registers (Fig.23 XOR1-XORn is the plurality of multipliers corresponding in number to the number of stages, the XOR with PN performs the product of its inputs) receiving an output from a stage of the at least two multiple stage shift registers as a first input; a tap weight shifter capable of circularly shifting tap weights (Fig.23 REG) coupled to a tap weight source (Fig.23 PN) to provide a second input to each multiplier; and an adder (Fig.23 ADD) for summing the multiplier outputs to provide a sum output (Fig.23 Aout). The new Ain inputs to the first stages of the SFREGs, and the input voltages contained in the stages of the

SFREG shifted toward the last stage and new sum is provided via ADD in response to the clocks (column 9 lines 55-65), at the CLK1 and CLK2 the ADD provides at least two sums.

Regarding **claims 4-5 & 19-20**, in FIG.23, Zhou et al. teaches the tap weights (PN) received by the tap weight shifter one bit wide and having a bit width that is no greater than a bit width of stage of the shift registers (column 9 lines 55-61 wherein the tap weights is one bit wide for each one stage of the SFREG).

Regarding **claim 33**, in Fig.3, Zhou et al. teaches a method of filtering digital data, comprising the steps of: a) shifting digital data into first and second/N multiple stage shift registers with L stages (Fig.3 R11-R1n & R21-R2n, N is at least 2, L is n); b) multiplying an output from each stage of the first and second/N multiple stage shift registers by an associated, respective tap weight to produce a plurality of products of R11-R1n on CLK0 (R11-R1n->XOR1-XORn); c) combining the plurality of products to form a sum (Fig.3 Aout); d) circularly shifting the tap weights (Fig.3 PN SREG, column 3 line 65 - column 4 line 3); e) repeating steps b and c for R21-R2n on CLK1 which is shifted by half a chip time from CLK0 at least once before step a loading new data.

Regarding **claims 35-36**, in Fig.3, Zhou et al. teaches a method of filtering digital data, comprising the steps of: a) shifting digital data into first and second/N multiple stage shift registers with L stages (Fig.3 R11-R1n & R21-R2n, N is at least 2, L is n); b) multiplying an output from each stage of the first and second/N multiple stage shift registers by an associated, respective tap weight to produce a plurality of products (R11-R1n->XOR1-XORn) on CLK0; c) combining the plurality of products to form a sum (Fig.3 Aout); d) circularly shifting the tap weights (Fig.3 PN SREG, column 3 line 65 - column 4 line 3); e) repeating steps b, c, and d N-2

times (when N=2 the steps c, b, and d do one time and repeat N-2/zero time) before loading the data; and f) repeating steps b and c for R12-R1n (R12-R1n->XOR1-XORn) on CLK1 which is shifted by half a chip time from CLK0 before the step a of loading the next data (column 3 lines 37-39); and repeating steps a through f for another new Ain.

Regarding **claims 38 & 46**, in Fig.3, Zhou et al. teaches digital filter /a receiver including a digital filter (column 1 lines 5-15 wherein the reception apparatus is the receiver), comprising: at least two (N>1) multiple stage shift registers (Fig.3 R11-R1n & R21-R2n); a tap changer adopt to store tap weights (Fig.3 SREG stores the PN); a plurality of multiplier corresponding in number to the number of stages in the at least two multiple stage shift registers (Fig.3 XOR1-XORn is the plurality of multipliers corresponding in number to the number of stages, the XOR with PN performs the product of its inputs) receiving an output from a stage of the at least two multiple stage shift registers as a first input the tap weight shifter (SREG) to provide a second input to each multiplier; and an adder (Fig.3 ADD) for summing the product outputs from each multiplier to provide a sum output (Fig.3 Aout); and filter generates two different sums: one for R11-R1n and one for R21-R2n as the PN shifted by CLKS correspondingly (column 3 line 65-column 4 line 3).

Regarding **claims 39-41**, in Fig.3, Zhou et al. teaches the tap changer SREG is a circular buffer and different configuration of the tap weights (PN sequences) is generated by shifting the tap weights; and the Din is loaded into the SREG in responding the CLKS which is synchronized with the clocks of shift registers, hence the Din is reloaded for a new data voltages values contained in the N stages of the shift registers after the N sums generated for previous N values in the N stages of the shift registers.

Regarding **claims 42-43**, in Fig.3, Zhou et al. teaches an input buffer (A/D of Fig.3) paralleizes an incoming serial data stream for input into the N stages of the shift registers, and N sums are generated by N shifts of the PN before another Ain shifted into N stages of the shift registers.

Regarding **claim 45**, in Fig.3, Zhou et al. teaches that the bit-width of PN is one (Fig.3), the bit-width of the datum is four (Fig.5 where the output of XOR is four bits), therefore, the bit-width of tap weight is smaller than the bit-width of each datum.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-3, 17-18, 34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US 6625205 B1) in view of Nishida (US 6229472 B1).

Regarding **claims 2-3, 17-18, 34 & 37**, in Fig.3 and Fig.23, Zhou et al. teaches the buffer A/D for receiving the input Ain, but does not explicitly specify it is a serial-input, parallel-output multiplier stage buffer for storing the N pieces of data prior to shifting into respective ones of the N multiple stage shift registers, however Nishida further s a serial-input, parallel-output multiplier stage buffer (FIG.5 13l-13m are multiplier stage buffer, Vin is the serial input, the outputs of 13l-13m are parallel-outputs) of A/D converter. As Zhou et al. using the A/D, at the

time of the invention, it would have been obvious to a person of ordinary skill in the art to have the serial-input, parallel-output multiplier stage buffer taught by Nishida implemented in Zhou et al.'s A/D to have an more efficient A/D converter with reduced power dissipation and occupied area (column 2 lines 54-58).

11. Claims 6-11 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US 6625205 B1) in view of Nishida (US 6229472 B1) as applied to claim 1 and claim 16 above, and further in view of Schilling (US 6366605 B1).

Regarding **claim 6**, Zhou et al. does not specify the software, however Schilling s the filter is implemented in software (column 2 line 64-column 3 line 5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the Zhou et al.'s filter in software taught by Schilling to have an improvement filter with reduced error rate (column 1 lines 35-45).

Regarding **claims 7-8**, Zhou et al. does not specify the integrated circuit/ASIC, however Schilling teaches the filter is implemented in IC/ASIC (column 2 line 64-column 3 line 5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the Zhou et al.'s filter in an IC/ASIC taught by Schilling to have an improvement filter with reduced error rate (column 1 lines 35-45).

Regarding **claims 9-11**, Zhou et al. does not specify the DSP/microcontroller/microprocessor, however Schilling teaches the filter is implemented in a DSP/software comprising microprocessor and microcontroller (column 2 line 64-column 3 line 5). At the time of the invention, it would have been obvious to a person of ordinary skill in the

art to implement the Zhou et al.'s filter in a DSP/microcontroller/microprocessor taught by Schilling to have an improvement filter with reduced error rate (column 1 lines 35-45).

Regarding **claim 32**, further Schilling teaches the receiver is the base station (Abstract). The modified/combined receiver (refer to rationale of claim 16) is the base station.

12. Claims 13-14, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US 6625205 B1) in view of Nishida (US 6229472 B1) as applied to claim 12 and claim 16 above, and further in view of Black et al. (6661833 B1).

Regarding **claims 13-14**, Zhou et al. teaches the shift register for weight source but not explicitly specify the ROM and RAM, however Black et al. teaches the ROM and RAM for PN sequence (column 11 lines 10-20). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the ROM/RAM taught by Black et al. for Zhou et al.'s PN to improve the acquisition of a CDMA system in a multiple system environment with different set of PN sequences (column 2 lines 24-40).

Regarding **claim 31**, further Black et al. teaches the receiver is the handset/mobile station (Abstract, column 2 lines 30-35). The modified/combined receiver (refer to rationale of claim 16) is a handset.

13. Claims 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US 6625205 B1) in view of Nishida (US 6229472 B1) as applied to claim 12 and claim 16 above, and further in view of Gronemeyer (US 6044105).

Regarding **claim 15**, Zhou et al. teaches the shift register for generating weights but not explicitly specify the processor, however Gronemeyer teaches the processor of code generator (column 11 lines 1-2 in the section Load GPS PN code, wherein the processor redesigned as the code generator). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the processor taught by Gronemeyer for generating weights to have a efficient receiver with low power and being fast (column 2 lines 50-55).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
November 7, 2004

YOUNG T. TSE
PRIMARY EXAMINER